9425 16 BITS MULTIPLEXED ANALOG INPUT MODULE

SPECIFICATIONS

Number of Analog Input Channels: 64 Differentials or Single Ended Multiplexed

Noise floor: at least -120dBv per √Hz over 85 kHz bandwidth

Channel Resolution: 16 bits

Digital Data Format: 16 bit 2's complement or offset binary

Conversion Rate: Programmable 300 kHz max.

Input Ranges: 0-5V, 0-10V, ±2.5V, ±5V, ±10V

Input Impedance: > 1Mohm

VME COMPLIANCE

Meets VME Specifications revision C.1 IEEE Std. 1014-1987

User programmable

A16:D16 DTB Slave or A24:D16 DTB Slave or A32:D16 DTB Slave

Address modifier code 29, 2D, 39, 3D, 09, or 0D HEX.

Short I/O or Standard I/O space covering 256K consecutive byte locations, base address configurable within 64K

I/O Space, 16M I/O Space, or 4G I/O Space.

Board size: 6U

Power Requirements

+5 Volts @ 250mA

+12 Volts @ 1A

Environmental

Operating Temperature: -40 to 85°C

Shock: 25g, 11ms on all axis

Storage Temperature: -60 to 125°C

The 9425 Analog Input Module offers the following features:

• Conversion rate software programmable signal, or timer
• Software Programmable Gain
• Optional Low Pass Filter
• Auto-scanning Mode
• 4K Word Data Buffer
• Single Channel Scan Mode
• Over-voltage Protection on Inputs
• Burst Mode triggered by software, external
• Software programmed interrupts
• The 9425 Analog Input Module offers a variety of operational modes. It is a drop in replacement for the VMIC VMIVME-3122 Analog to Digital Converter Board. While matching the register map and connector pinouts, the 9425 Module offers conversion rates 3 times faster than the VMIVME-3122 and a data buffer that is 4 times larger.
• In the auto-scanning mode all active channels are continuously scanned. A single scan mode causes all channels to be converted once. Another scan will be performed when the next trigger occurs. The random access mode allows for a selected channel to be continuously scanned.
• All scan modes may be triggered by either the software trigger, external trigger, or a programmable interval timer. The data from all conversions is stored in a dual port buffer. The user is informed that a scan cycle is completed by a data ready signal in a control register.
• Onboard arbitration prevents conflicts between VMEbus accesses and A/D converter accesses.